Temperature Aware Circuits: A Temperature Sensor for the Interconnect Layer

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ABSTRACT

In this paper, I describe the process of designing a temperature sensor for the interconnect layer in a modern microprocessor. This involves analyzing the interconnect layer, designing, simulating and evaluating the effectiveness of the temperature sensor circuit.

1.INTRODUCTION

Currently heat generation is a major concern of many chip designers, however todays methods focus on the device or silicon temperatures and do not factor in the interconnect layers. This is increasingly becoming a problem, since the current design rules do not take into account self heating and electromigration together, and thus fail to accurately model the heat being generated in the interconnect [1]. The reason these effects are of such concern is because they are both temperature sensitive and lead to failure of the circuit. Electromigration is the moving of conductors inside the metal that can cause higher resistance in the wire, or lead to an open circuit, it is also widely regarded as a major source of failure for interconnects [2]. I am proposing a temperature sensor to measure the interconnect temperature, giving chip designers real life temperature data to help them in future generations of design. The motivations for this project are: (1) to allow designers a better idea of the temperature of the interconnect, (2) to help develop methods to lengthen the lifetimes of microprocessor by limiting the effects of electromigration, (3) to provide a better microprocessor by facilitating predictions of where logical faults may occur due to excess heat, and (4) to limit the chance of thermal shutdown.

2.THE INTERCONNECT

Using the International Road-map for Semiconductor Technology (ITRS) is essential to make this sensor as accurate as possible. The ITRS contains a report exclusively for the interconnect layer and its parameter goals for the current technology, and those in the years to come. Although today it is common to find 11-12 metal layers in processors, I have only used data for 3 types of levels found in the ITRS (the local, semi-global and global levels). I chose to work in 130nm, 90nm, and 70nm technology to give a view of the kind of temperatures found and to be expected in the recent and the coming years. To model the interconnect layers I used a 3RC circuit with values obtained from the ITRS or the Predictive Technology Models (PTM) website. See figure 1 for an example of the 3 RC interconnect model used.

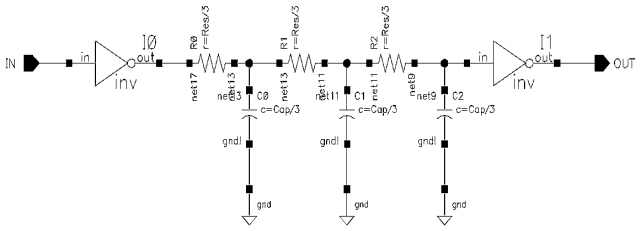

Figure 1. A 3RC distributed model of an interconnect. Shown are the values of Resistance as Res, and Capacitance as Cap.

After calculating the RC characteristics I found the optimal sizes. To obtain these I used eq 1 and 2. These equations provide the optimal size for line length and driver size [3].

$$L_{crit}=\sqrt{\frac{\frac{b}{a}\cdot r_o\cdot c_o\cdot(1+\frac{c_p}{c_o})}{r\cdot c}} \quad (1)$$

$$S_{opt}=\sqrt{\frac{r_o\cdot c}{c_o\cdot r}} \quad (2)$$

Where ro and co are Rout and Cout, c and r are line capacitance and Rline. Using these equations I produced the data found in table 1.

Table 1a. Optimal Size Data for 130nm technology node.

Layer	Lcrit (um)	Sopt	Rout (Ohms)	Rline (Ohms)	Rout/Rline
Local	130.23	63.02	81.68	124.35	0.657
Semi Global	174.24	63.44	61.47	93.58	0.657
Global	275.98	72.50	36.44	55.48	0.657

Table 1b. Optimal Size Data for 90nm technology node.

Layer	Lcrit (um)	Sopt	Rout (Ohms)	Rline (Ohms)	Rout/Rline
Local	88.26	66.44	90.88	141.01	0.645
Semi Global	98.13	66.58	81.85	126.99	0.645

Global	156.56	81.56	44.85	69.58	0.645

Table 1c. Optimal Size Data for 70nm technology node.

Layer	Lcrit (um)	Sopt	Rout (Ohms)	Rline (Ohms)	Rout/Rline
Local	69.35	66.31	94.51	147.08	0.643
Semi Global	74.11	66.69	87.83	136.69	0.643
Global	117.36	81.56	48.26	75.11	0.643

In the tables Lcrit is the optimal size of an interconnect wire connecting two drivers shown in microns. Sopt is the optimal size of the driver in multiples of the technology node. Rout and Rline are the resistances of the driver (seen from the line) and the line both shown in Ohms. Finally I have included the ratio to show the difference between technology nodes. By using real data provided by the ITRS, and PTM and calculating the optimal sizes we are given a good idea about the actual size of interconnects in various technologies. This will ultimately give us an idea about how to size the temperature sensor effectively. The interconnect temperature can be found by using the self consistent equation [1], shown in equation 3.

$$r = \frac{4 \cdot j_0^2 \cdot e^{\frac{Q}{k_B \cdot T_m}}}{e^{\frac{Q}{k_B \cdot T_{ref}}}} \frac{t_{ins} \cdot t_m \cdot W_m \cdot p_m}{(T_m - T_{ref}) \cdot K_{ins} \cdot W_{eff}} \quad (3)$$

In equation 3 r represents the duty cycle (javg^2 / jrms^2), j0 is the design rule current density stress, Q is the activation energy, kB is Boltzmans constant, Tm is the new temperature of the metal, Tref is the reference temperature of the metal, tins is the dielectric thickness, tm is the metal thickness, Wm is the width of the metal, pm is the resistivity of the metal (based on Tm), and Kins is the dielectric thermal constant [1]. Using this equation and the values found we can calculate temperature of the interconnect based on the duty cycle. This yields figure 2, a graph of temperature Vs duty cycle for different technology nodes.

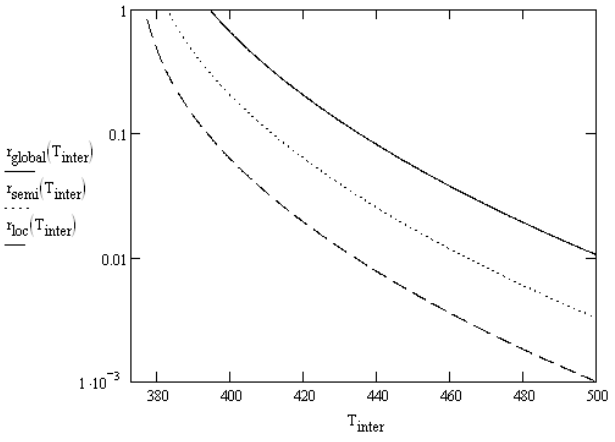

Figure 2. Self consistent equation (3) on 90nm for global, semi global and local interconnect layers. The Y-axis is the duty cycle, and on the X-axis temperature is shown in K.

According to the equation and graph we find that for these technology nodes the interconnect temperature can reach reasonably high levels.

3.THE SENSOR

Frequency Based

The temperature sensor used will be based on detecting the frequency of some oscillations. This will be achieved by placing a length of wire near the interconnect temperature to be measured, and having a circuit determine the change in resistance by measuring the change in frequency of the oscillations due to an increased resistance, caused by higher temperatures in the wire. The goal is to obtain a circuit that is insensitive to change in temperature, but have a wire that is very sensitive to changes in temperature, thereby allowing the sensing circuit to measure the interconnect temperature accurately even when it is being heated by the its surroundings. It is also important to use an effective temperature sensor. An effective temperature sensor involves the following: (1) linearity, providing a linear graph over the range of resistances and temperatures I will be interested in, (2) sensitivity, the ability to track small changes in temperature, (3) easy to calibrate, and (4) easy to measure.

Modified Ring Oscillator

By placing the wire inside a ring oscillator the oscillation frequency will change. I tested a few designs of ring oscillators, and found the one shown in figure 3 to be the best for simulation.

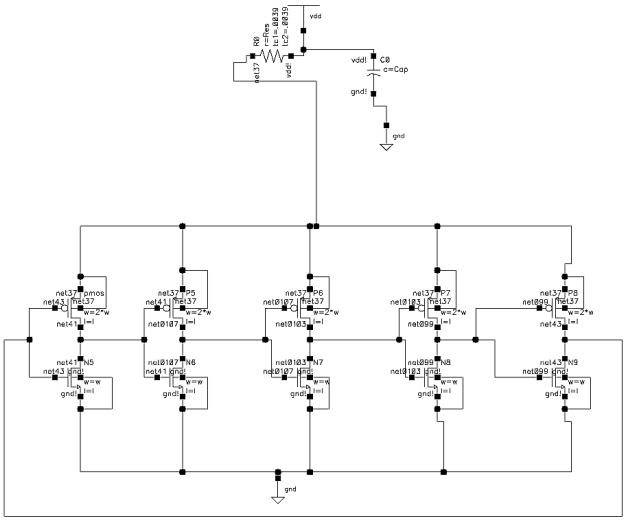

Figure 3. Modified Ring Oscillator, shown with 5 inverters and the wire (R0 and C0) placed between Vdd and the inverters.

By placing the wire between Vdd and the transistors we hoped to affect the speed of the inverters drastically with small changes in resistance (R0). In table 2 and figure 4 you can see some of the results obtained.

Table 2a. This shows results obtained through simulation in 90nm technology, a length of 150 micron global interconnect wire for temperatures between 50 and 200 degrees C varied in

the simulator (for the whole circuit). Current and voltage (Ipeak, Irms, Iavg, Vrms) measurements made through the resistor R0.

Temp. (C)	50	75	100	125	150	175	200
R0 (Ohm)	53.66	61.16	66.66	73.16	79.66	86.16	92.66
Freq. (Ghz)	3.754	3.079	2.555	2.151	1.841	1.608	1.448
Ipeak (uA)	60.019	47.904	38.339	30.634	25.080	20.772	17.480
Irms (uA)	43.363	35.100	28.504	23.401	19.509	16.468	14.103
Iavg (uA)	42.046	34.111	27.810	22.920	19.176	16.232	13.934
Vrms	0.002	0.002	0.002	0.002	0.002	0.001	0.001
Vdd	0.998	0.998	0.998	0.998	0.998	0.999	0.999
Prms (nW)	100.90	74.12	54.16	40.06	30.32	23.37	18.43
r	0.94	0.94	0.95	0.96	0.97	0.97	0.98

Table 2b. This shows results obtained through simulation in 90nm technology, a length of 150 micron global interconnect wire for temperatures between 50 and 200 degrees C varied by manually changing the value of R0 (not the whole circuit). Current and voltage (Ipeak, Irms, Iavg, Vrms) measurements made through the resistor R0.

Temp. (C)	50	75	100	125	150	175	200
R0 (Ohm)	53.66	61.16	66.66	73.16	79.66	86.16	92.66
Freq. (Ghz)	4.529	4.527	4.525	4.523	4.521	4.519	4.517
Ipeak (uA)	71.904	71.796	71.690	71.617	71.581	71.451	71.315
Irms (uA)	52.313	52.273	52.232	52.190	52.145	52.098	52.045
Iavg (uA)	50.786	50.752	50.718	50.681	50.641	50.601	50.552
Vrms	0.003	0.003	0.003	0.004	0.004	0.004	0.005
Vdd	0.997	0.997	0.997	0.996	0.996	0.996	0.995
Prms (nW)	146.85	164.39	181.86	199.27	216.60	233.91	250.99
r	0.94	0.94	0.94	0.94	0.94	0.94	0.94

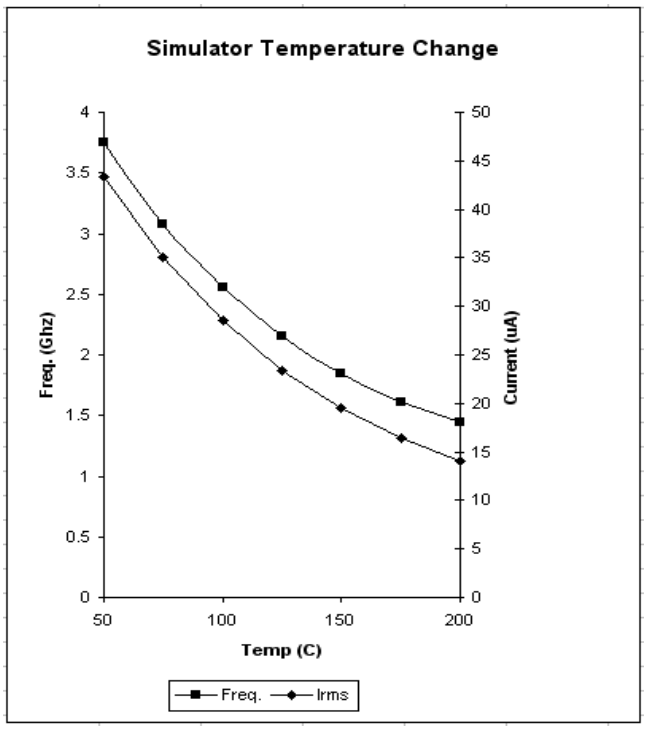

Figure 4a. This graph shows results obtained through simulation in 90nm technology, a length of 150 micron global interconnect wire for temperatures between 50 and 200 degrees C varied in the simulator (for the whole circuit).

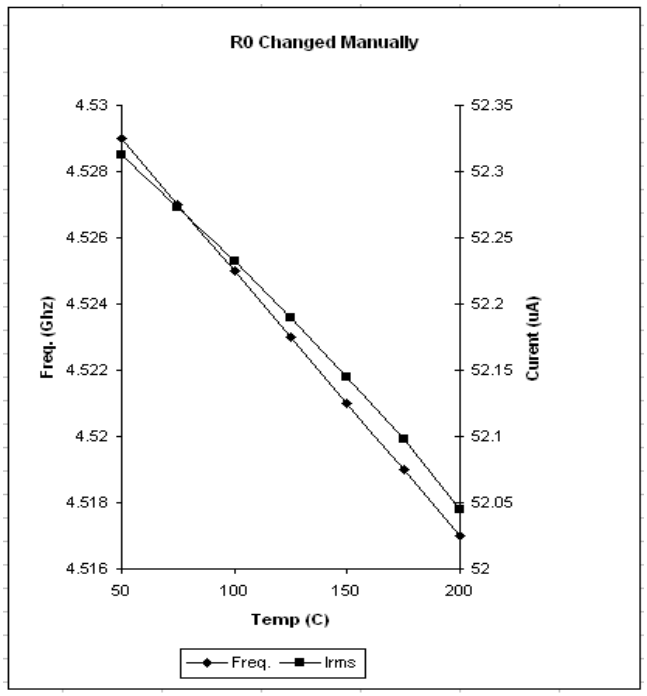

Figure 4b. This graph shows results obtained through simulation in 90nm technology, a length of 150 micron global interconnect wire for temperatures between 50 and 200 degrees C varied by manually changing the value of R0 (not the whole circuit).

This is the data for only the global 90nm interconnect, I have also simulated the other layers and technology nodes, however they all have the same shortcomings. After analyzing the data, this ring oscillator is found to be ineffective as a temperature sensor. The reasons behind this are (1) the inability to affect Vdd without drawing too much current, (2) the sensitivity of the ring oscillator to temperature change, and (3) the high frequency and not enough change in frequency based on changes in temperatures. The failure based on reason (1) might be remedied by using a larger wire, or increased capacitance, however in the shown tables for 90nm, a 1000um wire would still only have 444 Ohm resistance at 100C, and using a larger capacitor would take up too much area. Also using more resistance would lead to self heating in the wire affecting the temperature calculations of the interconnect layer. Reason (2) shows the weakness in choosing a ring oscillator circuit, and is shown by comparison of Figures 4a and 4b, there is too much change when comparing the change in frequencies based on the first and second graphs. Shortcomings causing reason (3) might be overcome with higher capacitance, and larger resistance, but area is still prohibitive. All in all, the ring oscillator circuit is not a good choice for a temperature sensor.

An RC Oscillator

To overcome the shortcomings of the ring oscillator I plan to use an RC oscillator circuit. This circuit will use a transconductance amplifier in conjunction with a length of wire and some extra resistance and capacitance. These changes should enable the circuit to function more independently of temperature, save the wire placed near the interconnect layer to be measured. I am in the process of testing available designs and choosing one to suit my needs best.

4.CONCLUSIONS

After spending much time designing and simulating the ring oscillator circuit it is apparent that it will not work as intended. The failure to account for the shortcomings already discussed caused my inability to simulate a successful temperature sensor for this class. More importantly it shows me how important the design phase is, and taking into account things you might not have thought would be a problem to save wasting your time simulating something that you could already know will fail.

5.ACKNOWLEGEMENTS

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6.REFERENCES

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